Claim Amendments

1-39. (canceled)

40. (new) A test structure for testing the sufficiency of tunnel opening sizes in a non-volatile memory cell, comprising:

multiple individually programmable write paths aligned substantially in parallel;

multiple floating gates aligned substantially in parallel and aligned substantially perpendicularly to the multiple write paths, the floating gates overlapping the multiple write paths to form an array of intersecting areas;

an array of tunnel openings formed in the intersecting areas and between the floating gates and write paths, with the tunnel openings formed over a same write path being of substantially a same size and with the tunnel openings formed over different write paths being of different sizes; and

a read path coupled to the floating gates and operable to detect a programmed write path if the tunnel openings formed over the programmed write path are of sufficient size to successfully couple the floating gates to the programmed write path.

41. (new) The test structure of claim 40, including a control path operable to program and erase the floating gates in parallel.

42. (new) The test structure of claim 40, wherein the read path is coupled to all of the floating gates.

43. (new) The test structure of claim 40, wherein the test structure is located on a semiconductor wafer.

44. (new) A test structure for testing the sufficiency of tunnel opening sizes in a non-volatile memory cell, comprising:

N write paths aligned substantially in parallel, each of the write paths beings individually programmable;

M floating gates, each of the floating gates overlapping each of the multiple write paths to form a N column-by-M row array of intersecting areas;

an N column-by-M row array of tunnel openings formed in the intersecting areas and between the floating gates and write paths, with the tunnel openings in each array column being of a same size and the tunnel openings in each array row being of different sizes; and

a read path coupled to the M floating gates and operable to detect a programmed write path if the tunnel openings formed over the programmed write path are of sufficient size to successfully couple the M floating gates to the programmed write path.

45. A test structure on a semiconductor wafer for testing the sufficiency of tunnel opening sizes in a non-volatile memory cell, comprising:

a plurality of individually programmable write paths aligned substantially in parallel;

a plurality of floating gates aligned substantially in parallel and intersecting each of the write paths;

an array of tunnel openings formed between the intersections of the write paths and floating gates, with the tunnel openings corresponding to a same write path being of a same size and with tunnel openings corresponding to different write paths being of different sizes; and

a read path coupled to the floating gates and operable to detect a programmed write path if the tunnel openings corresponding to the programmed write path are of sufficient size to successfully couple the floating gates to the programmed write path.